REMARKS

In an Office Action dated July 14, 2004, and the subsequent advisory action mailed October 22, 2004, the Patent Office finally rejected claims 1-31 under 35 U.S.C. §103. Applicant adds claim 32. Applicant does not cancel any claims or amend any claims. Accordingly, claims 1-32 are pending.

I. Request for telephonic interview

In accordance with a conversation with the Examiner prior to the preparation of the Request for Continued Examination, Applicant requests that the Examiner contact the Applicant prior to the preparation of the first Office Action to conduct an interview related to the rejection of the claims under 35 U.S.C. §103. Applicant respectfully reminds the Examiner that he indicated during a telephone conversation that he would be amenable to such an interview.

II. Claims Rejected Under 35 U.S.C. § 103

Claims 1-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,651,163 issued to Kranich, et al., (hereinafter "Kranich") in view of U.S. Patent No. 6,425,039 issued to Yoshioka, et al. (hereinafter "Yoshioka"). Applicant disagrees for the following reasons.

To establish a *prima facie* case of obviousness, the Examiner must show that the cited references teach or suggest each of the elements of a claim. In regard to claims 1, 12, and 21, these claims include the elements of "executing a number of instructions at an address within a common interrupt handling vector address space ... wherein the number of instructions cause the processor to determine an identification of the processor based on a query that is internal to the processor." In the advisory action mailed October 22, 2004, the Examiner cites column 22, line 39 through column 23, line 28 as teaching these elements of claims 1, 12 and 21. The Applicant

has previously argued that Kranich does not teach these elements of these claims and requested in each instance that the Examiner clarify where in Kranich these elements are taught. In the last three communications from the Examiner, the Examiner cited three different sections as teaching these elements but did not provide any discussion of these sections to clarify how the cited sections teach the elements of these claims.

The sections of Kranich the Examiner cites in the Advisory Action, in fact, do not teach executing instruction within a common interrupt handling vector that cause a processor to determine its identification using a query that is internal to the processor as argued by the Examiner. The cited section of Kranich column 22, line 39 through column 23, line 28 discusses dynamic processor numbering and exception handling. This section discusses the use of a mapping table 350 in a multiprocessor environment that is used to save the state of a processor handling an exception as well as the state of other processors. See column 23, lines 5-10.

Applicant reminds the Examiner that the mapping table 350 is not a part of any processor. See Figure 3A of Kranich. After saving the state of each of the processors in the mapping table, "the processor which generated the exception then handles the exception." See Kranich, column 23, lines 10 and 11. The remainder of the paragraph then goes on to describe the restoration of the state to each of its processors. See col. 23, lines 11-28. Thus, the cited section of Kranich makes no mention of the execution of an instruction during exception handling that requires a processor to check its identification.

Further, the same section makes clear that in general when multiprocessor instructions are executed that contain a processing number, it is necessary to access a table external to the processor, i.e., mapping table 350, to determine the actual physical processor to which the instruction is related. See Kranich, column 23, lines 23-28. Thus, Kranich does not teach "a

number of instructions at an address within a common interrupt handling vector address space" that "cause the processor to determine an identification of the processor based on a query that is internal to the processor" as claimed in claims 1, 12 and 21.

Further, the Examiner has failed to consider the claimed invention as a whole. See MPEP § 2141, describing the basic considerations which apply to obviousness rejections. The Examiner continues to argue that Kranich teaches a process that queries internal and external registers to determine the identity of the processor. However, the claims recite executing instructions *within a common interrupt handling vector* where these instructions *cause a processor to determine identification of the processor with an internal query.* The Examiner has not set forth any part of Kranich that teaches an instruction from within a common interrupt handler that causes identification of the processor with an internal query. In fact, the Examiner admits that Kranich does not teach or suggest the use of common interrupt handling vector. See page 7, paper number 7. Thus, Kranich cannot teach an instruction within a common interrupt handler that causes an internal query to identify the processor. Therefore, the Examiner has failed to establish that Kranich teaches each of the elements of claims 1, 12 and 21.

The Examiner has not identified and Applicant has been unable to discern any part of Yoshioka that cures these defects of Kranich. Specifically, the Examiner has not identified any part of Yoshioka that teaches an instruction within a common interrupt handling vector that causes a processor to determine its own identification. Thus, the Examiner has not established that Kranich in view of Yoshioka teaches or suggests each of the elements of claims 1, 12 and 21. In the advisory action, the Examiner responds to Applicant's argument that Yoshioka does not cure the defects of Kranich by discussing Yoshioka teaching a common interrupt handler. The Examiner misses the point of Applicant's arguments. Applicant argues that neither Kranich

nor Yoshioka teach an instruction in a common interrupt handler that causes an executing processor to determine its own identity. Thus, Kranich and Yoshioka combined do not teach or suggest each of the elements of claims 1, 12 and 21.

The Examiner has improperly combined Yoshioka with Kranich. Kranich utilizes a thread control device and mapping table and a dynamic processor number scheme to coordinate the handling of interrupts and exceptions in a multiprocessor environment. Combining the system of Kranich with the common interrupt vector system of Yoshioka changes the principle of operation of Kranich and thus makes the combination improper. See MPEP § 2143.01, "The Proposed Modification Cannot Change The Principle Of Operation Of A Reference." Also, the Examiner has failed to provide a rational explanation as to how their cited references suggest the desirability of the proposed modification of Kranich. See MPEP § 2143.01, "The Prior Art Must Suggest The Desirability of the Claimed Invention." Kranich teaches a system that is already capable of handling interrupts and exceptions in a multiprocessor environment. The Examiner has not provided any reference to any part of Kranich or Yoshioka that teaches the desirability of modifying Kranich to include a common interrupt handling vector. Thus, the Examiner has failed to establish *prima facie* case of obviousness for independent claims 1, 12 and 21.

In the Advisory Action, the Examiner responds to the Applicant's argument that Kranich was improperly combined by stating that "the test for obviousness" is "what the combined teachings of the references would have suggested to those of ordinary skill in the art" and cites *In re* Keller 208 USPQ 871, 881 (CCPA 1981) and In re Young, 18 USPQ 2d 1089, 1981 (Fed. Cir. 1991) in support of this position. The section of the MPEP that the Examiner relies upon for these citations, namely MPEP § 2145 (III) specifically states that the holding of *In re* Keller does not mean that a claimed combination that changes a principle of operation of a primary reference

is proper. See the last paragraph of this section that cites MPEP § 2143.01. This is exactly the argument of the Applicant. Thus, the Examiner's statements are non-responsive to the arguments set forth by the Applicant.

Further, the Examiner has not responded to the Applicant's argument that the Examiner has failed to provide a rational explanation as to how the cited references suggest the desirability of the proposed modification of Kranich. See MPEP § 2143.01, "The Prior Art Must Suggest The Desirability of the Claimed Invention." Kranich teaches a system that is already capable of handling interrupts and exceptions in a multiprocessor environment. The Examiner has not provided any reference to any part of Kranich or Yoshioka that teaches the desirability modifying Kranich to include a common interrupt handling vector. The holding of *In re* Keller is a general statement that the combination of references is based on what would be suggested to those of ordinary skill in the art. The analysis of what would be suggested to one of ordinary skill in the art includes discerning whether or not it would be desirable to combine the references. Applicant notes that "in determining the propriety of the Patent Office case for obviousness in the first instant, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the proposed substitution, combination, or other modification," *In re Linter*, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). The Examiner has not set forth such a rationale. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 1, 12 and 21.

In regard to claims 2-6, 13-16 and 22-26, these claims depend from independent claims 1, 12, and 21 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to claims 1, 12 and 21, these claims are not obvious over Kranich in view of

Yoshioka. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

In regard to claims 8, 17 and 28, these claims include the elements of executing "a number of instructions at an address within the common interrupt handling address space of the same memory, wherein a number of instructions cause a processor to read a bit within an internal register to determine an identification of a processor and a multiprocessor system. The Examiner cites the same section of Kranich as discussed above in regard to claims 1, 12 and 21. Column 22, line 39 through column 23, line 28. For the reasons set forth above in regard to claims 1, 12 and 21, this section of Kranich does not teach or suggest executing a set of instructions that are within a common interrupt handler vector where one of the instructions from the common interrupt handling vector cause a processor to determine its identification based on a query that is internal to that processor including reading a bit within an internal register of that processor. Further, the sections of Kranich cited by the Examiner make no mention of reading bits in an internal register. Thus, the Examiner has failed to establish that Kranich teaches each of the elements of claims 8, 17 and 28 as set forth above in regard to independent claims 1, 12 and 21.

Yoshioka does not cure these defects of Kranich and is not properly combined with Kranich. The Examiner has not indicated any part of Yoshioka that teaches these elements of claims 8, 17 and 28. The Examiner relies on the same rationale for combining Yoshioka with Kranich in relation to claims 8, 17 and 21 as presented in regard to claims 1, 12 and 21. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 8, 17 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

In regard to claims 9-11, 18-20 and 29-31, these claims depend from independent claims 8, 17 and 28, respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to claims 8, 17 and 28, these claims are not obvious over Kranich in view of Yoshioka. Applicant again reminds the Examiner that the Examiner has not set forth a basic argument for each of these claims and therefore has not set forth a *prima facie* case of obviousness for these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

Claims 1, 8, 12, 17, 21 and 28 stand rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent Application Number 2002/00713154 by Brenner, Jr., et al. (hereinafter "Brenner") in view of U.S. Patent Number 6,006,247 issued to Browning, et al. (hereinafter "Browning"). Applicant respectfully disagrees for the following reasons.

Claims 1, 12 and 21 include the elements of executing "a number of instructions at an address within a common interrupt handling vector address base . . . wherein the number of instructions caused the process to determine the identification of the processor based on a query that is internal to the processor." In a previous Office Action, Paper No. 7, December 4, 2003, the Examiner admitted that Brenner did not teach or suggest these elements and relied on Browning, specifically arguing that the processor accessing a global memory depicted in Figure 2 taught these elements of the claims. In the Office Action mailed July 14, 2004, the Examiner changed his position and cited column 1, line 2 through column 3, line 11 of Browning as teaching these elements. Now the Examiner again changes his position and relies on Brenner, which he previously admitted did not teach these elements and cites paragraphs 9-11 of Brenner as teaching these elements of claims 1, 12 and 21. Applicant has reviewed the cited sections of Brenner but has been unable to discern any part therein that teaches instructions in and address

space within a common interrupt handling vector that causes a processor to determine an identification of the processor as claimed. Brenner relates to a uniprocessor system. Applicant cannot understand how Brenner teaches identifying a processor or how any of the teachings in paragraphs 9-11 could imply identifying a processor, which in a uniprocessor system such as Brenner's is unnecessary.

Similarly, claims 8, 17 and 28 include the elements of "a number of instructions at an address within the common interrupt handling address base of the same memory, wherein the number of instructions cause the processor to read a bit within an internal register to determine an identification of a processor in a multiprocessor system." The Examiner cites paragraphs 4-7 of Brenner as teaching these elements of the claims. Again, Brenner teaches a uniprocessor system and Applicant has been unable to discern any part of paragraphs 4-7 that teach or suggest these elements of claims 8, 17 and 28.

The Examiner offers the same argument based *In re* Keller in support of a combination of Brenner and Browning. Applicant's arguments set forth above in regard to the combination of Yoshioka and Kranich as well as the Applicant's arguments previously set forth in response to the Final Office Action have not been addresses by the Examiner. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for claims 1, 8, 12, 17, 21 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 1, 8, 12, 21 and 28 are requested.

III. Interpretation of the Claims

In the Advisory Action mailed October 22, 2004, the Examiner cites page 13, lines 10-18 of the present application and states "Since, applicant's claims contain broadly claimed subject matter, it clearly reads upon the Examiner's intepretation of these actions." While Applicant

does not disagree that the language of the claims should be given the broadest reasonable interpretation, the Examiner appears to have ignored the plain meaning of the claims, failed to interpret the claims as a whole and read the claims so broadly as to render the language of the claims as having no meaning. It is unclear to Applicant how he can construct a claim to overcome the prior art because the Examiner appears to be interpreting the claims so broadly as to render any limiting language meaningless. Further, the Examiner has not set forth how the Examiner interprets the language of the claims of the application and has not clearly set forth how that language is read on by the references. This makes it difficult, if not impossible, for the Applicant to have a meaningful discussion of the claims or to amend them to overcome prior art rejections.

IV. New Claim

Applicant submits herewith a new claim 32 based on the Examiner's proposed modification of claims provided in the Advisory Action. Applicant has altered the language provided by the Examiner to remove factually incorrect non-supported elements.

Conclusion

In view of the foregoing, it is believed that all claims now pending, namely claims 1-32, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Dated: 11/15, 2004

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 15, 2004.

Lillian E. Rodriguez 11-15-04

Lillian E. Rodriguez November 15, 2004